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10/766,320	01/29/2004	Marcelo Krygier	QIM 2006 P 50708 US	1221
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SLATER & MATSIL, L.L.P. 17950 PRESTON ROAD SUITE 1000 DALLAS, TX 75252			DOAN, DUC T	
		ART UNIT	PAPER NUMBER	
		2188		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/766,320	KRYGIER, MARCELO	
	Examiner	Art Unit	
	DUC T. DOAN	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 28 March 2008.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-24 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____ .	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/28/2008 has been entered.

Claims 1-24 have been presented for examination in this application.

Claims 1-24 are rejected.

Applicant's remarks filed 2/28/2008 have been fully considered but they are mooted in view of new ground(s) of rejection applied with new reference(s) found.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-8, and 10-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lakhani et al (US 2003/0126385), in view of SanDisk Secure Digital Card product manual, version 1.9, herein SanDisk Secure Digital Card product manual, version 1.9, herein SD, (SanDisk Corp, December 2003).

As in claim 1, Lakhani discloses a method for operating a non-volatile memory device comprising:

receiving a command that includes an address argument comprising a plurality of address bits, one or more of address bits comprising unused bits and any remaining bits providing an address for a location in the non-volatile memory device (Lakhani's control bits and address bits corresponds to the claim's address argument for a memory access command. Because the control bits do not contain address bits of memory device such as bits A [22:0] therefore the control bits are unused bits of an address argument as claimed).

using the one or more unused bits of the address argument of the command as an addressing mode field to determine whether said address argument is a byte address argument or a block address argument (Table A, paragraph 75, C1,C2 bits used as a first mode/ byte addressing mode; paragraph 69; paragraph 76 discloses C1,C2 bits being used to determine a second mode, corresponding to the claim's block mode, in which an operation occurs for data in blocks of memory devices, see paragraph 70);

the remaining bits provide a byte address when the address argument is a byte address argument and the remaining bits provide a block address when the address argument is a block address argument (Lakhani's paragraphs 69,70,76, the remaining bits

A are provided/used in either addressing mode), Lakhani does not disclose the block address having the same number of bits as the byte address. However, SD discloses a method accessing block of data using commands that are byte addressable (see SD's 1.5.10.4). It would have been obvious to one of ordinary skill in the art at the time of invention to include the block mode accessing data with byte addressable as suggested by SD in Lakhani's system thereby further allowing accessing data of memory being accessed in block mode with additional byte addressing capability.

As in claims 2-3, Lakhani discloses determining that the address argument is the byte address argument when the addressing mode field is zero (claim 2; Lakhani's paragraph 75 discloses the C1, C2 having value 0 for first mode/byte mode operation); determining that the address argument is the block address argument when the addressing mode field is one (claim 3; Lakhani's paragraph 76 discloses C1 having value of 1 for second mode/block mode operation).

As in claim 4, Lakhani discloses accessing a byte address within a memory unit according to the byte address argument if said address argument is a byte address argument (claim 4, Table A, paragraph 75, C1,C2 bits used as a byte addressing mod, paragraph 69).

As in claim 5, Lakhani discloses accessing a block address within a memory unit according to the block address argument if said address argument is a block address argument (Table A, paragraph 76, C1, C2 bits used as block address mode, in which an operation occurs for data in blocks of memory device, see paragraph 70).

As in claims 6-7, Lakhani does not disclose the significant bit aspect. However, it is known that these unused bits can be designated as least significant bits of the address

arguments or the most significant bits of the address argument as desired, for example, the designation can be based on whether the endianess of the associating logic operates on the data.

As in claim 8, Lakhani discloses an apparatus comprising: a non volatile memory unit (Lakhani's Fig 2: #16 , paragraph 13), a controller adapted to determine whether an addressing mode to access said memory unit is a byte addressing mode or a block addressing mode and to send a command to access data within said memory unit according to said addressing mode (Lakhani's Fig 2, associating controlling logic such as controller engine #41, predecoder #50), wherein: in the byte addressing mode, address bits of an address argument of the command provide a byte address, and in the block addressing mode, said address bits of the address argument of the command provide a block address (Lakhani's paragraphs 70,76 bits such as a[22:0],E[7:0] etc.. provide an address for corresponding addressing modes), Lakhani does not disclose the block address having the same number of bits as the byte address. However, SD discloses a method accessing block of data using commands that are byte addressable (see SD's 1.5.10.4). It would have been obvious to one of ordinary skill in the art at the time of invention to include the block mode accessing data with byte addressable as suggested by SD in Lakhani's system thereby further allowing accessing data of memory being accessed in block mode with additional byte addressing capability.

As in claim 10, Lakhani does not, however SD discloses said memory unit is a secure digital (SD) memory card. It would have been obvious to include SD teaching in Lakhani's system for the same reason stated above.

As in claim 11, Lakhani disclose a non-volatile memory unit (Fig 2: 16); and a controller to determine whether an address mode to access said memory unit is a byte addressing mode or a block addressing mode and to send a command to access data within said memory unit according to said addressing mode. Lakhani's Table A discloses an addressing scheme having addressing mode bit C1 to determine the addressing mode of the address A[31:0]. Lakhani does not expressly disclose the size of the command using with the above address scheme as being 48 bits and or the addressing mode bit is the ninth bit of a 48-bit command. However, SD discloses a 48 bit command is used for access a memory device such as secure digital memory device (SD's 4-3). SD further discloses a method accessing block of data using commands that are byte addressable (see SD's 1.5.10.4). It would have been obvious to one of ordinary skill in the art at the time of invention to include the block mode accessing data with byte addressable as suggested by SD in Lakhani's system thereby further allowing accessing data of memory being accessed in block mode with additional byte addressing capability. Regarding the claim's limitation the ninth bit of a 48-bit command. Lakhani and SD do not explicitly disclose the specific bit location. However, it is obviously, depending how many commands are needed for a particular memory system and what protocol being used, the size of the command can be varied, additional information can be included/removed in the command and thus information such as addressing mode, address bits etc.. can be arraigned in the command at various bit locations specifically as desired.

Claim 12 is rejected based on the same rational as of claim 11. Examiner further notes that the addressing mode associating with the 40 bits instead of associating with the

9th bit as recited in claim 11 is due to reverse labeling the bits of the 48 bit command entity, which is known in the art as endiness of data.

As in claim 13, Lakhani discloses a storage medium having stored thereon instructions that when executed by a computing platform functionally associated with a non-volatile memory device result in (Lakhani Fig 2: #16 non volatile memory of a flash memory system, paragraphs 5,17 providing instructions for a standard operating system being executed by a computing platform/host processor that result in) using one or more bits of a command as an addressing mode field to determine whether an address argument of the command is a byte address argument or a block address argument (Lakhani's page 7 table A, paragraph 75 discloses C1,C2 bits being used to determine the first mode, address bits being interpreted as byte address for an operation in a memory device, see paragraph 69; Lakhani's paragraph 76 discloses C1,C2 bits being used to determine the second mode, corresponding to the claim's block mode, in which an operation occurs for data in blocks of memory devices, see paragraph 70), wherein: when said address argument is a byte address argument, address bits of the address argument provide a byte address, and when said address argument is a block address argument, said address bits of the address argument provide a block address (Lakhani's paragraphs 70,76 bits such as a[22:0],E[7:0] etc.. provide an address for corresponding addressing modes), Lakhani does not disclose the block address having the same number of bits as the byte address. However, SD discloses a method accessing block of data using commands that are byte addressable (see SD's 1.5.10.4). It would have been obvious to one of ordinary skill in the art at the time of invention to include the block mode accessing data with byte

addressable as suggested by SD in Lakhani's system thereby further allowing accessing data of memory being accessed in block mode with additional byte addressing capability.

As in claim 14, Lakhani discloses using one or more unused bits of the address argument as the addressing mode field. Lakhani's paragraph 84 discloses a method for operating non-volatile devices using bits C1, C2 that is not being used as addressing bits.

Claim 15 rejected based on the same rationale as of claim 2.

Claim 16 rejected based on the same rationale as of claim 3.

As in claim 17 Lakhani further discloses wherein the addressing mode field comprise one or more unused bits of the address argument of the command (Lakhani's control bits and address bits corresponds to the claim's address argument. Because the control bits do not contain address bits of memory device such as bits A [22:0] etc..therefore the control bits are unused bits of an address argument as claimed).

As in claim 18, Lakhani disclose a method for operating a non-volatile memory device, the method comprising: receiving a command that includes an address argument comprising a plurality of address bits and an addressing mode field (Lakhani's paragraphs 73, 76-77, Table A control C1, C2 and address bits A[22:0], E[7:0]), the addressing mode field indicating whether the address argument contains a byte address or a block address (Lakhani's control bits and address bits corresponds to the claim's address argument, Lakhani's paragraphs 73,76-77); and

If the addressing mode field indicates that the address argument contains a byte address, using the address bits to address a byte of data; or if the addressing mode field indicates that the address argument contains a block address, using the address bits to

address a block of data (Lakhani's paragraphs 73, 76-77 control C1, C2 and address bits

A[22:0], E[7:0] provides proper address for a selected address mode),

Lakhani does not disclose the block address having the same number of bits as the byte address. However, SD discloses a method accessing block of data using commands that are byte addressable (see SD's 1.5.10.4). It would have been obvious to one of ordinary skill in the art at the time of invention to include the block mode accessing data with byte addressable as suggested by SD in Lakhani's system thereby further allowing accessing data of memory being accessed in block mode with additional byte addressing capability.

As in claim 19, Lakhani does not, however, SD discloses wherein the command further comprises a start bit, a transmission bit, a command code, a plurality of CRC, checksum bits and an end bit (see SD 4-3). It would have been obvious to include SD teaching in Lakhani's system for the same reason stated above.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lakhani et al (US 2003/0126385), SanDisk Secure Digital Card product manual, version 1.9, herein SD, (SanDisk Corp, December 2003) as applied above, and further in view of Zer et al (US 2005/0055479).

As in claim 9, Lakhani discloses wherein said memory unit is a multi media card (MMC) (claim 9) Lakhani and SD do not expressly disclose the memory is a multi media card or secure digital card. However, Zer's paragraph 6 discloses systems using the removable storage device such as MMC and SD cards. It would have been obvious to one of ordinary skill in the art at the time of invention to use the removable memory cards, for

example MMC and SD cards, as suggested by Zer in Lakhani's system modified by SD thereby further providing secure, light weight, efficient data transferring storage media for various systems such as PDA, cellular telephones (see Zer's paragraphs 6-7).

Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lakhani et al (US 2003/0126385), SanDisk Secure Digital Card product manual, version 1.9, herein SD, (SanDisk Corp, December 2003) as applied above, and further in view of PCI specification revision 2.2 (herein PCI Specification).

As in claims 20-22, Lakhani and SD do not expressly disclose the claims' detail associating with the addressing mode. However, PCI specification discloses wherein the addressing mode field comprises only a single bit (claim 20, PCI specification's page 202 AD[0]), the address argument contains a byte address when the addressing mode field contains zero (claim 21, PCI specification's page 202, I/O space address mode with AD[0] is zero), the addressing mode field comprises a bit of the address argument (claim 22, PCI specification's page 202, AD[0] comprises a bit of the address argument). It would have been obvious to one of ordinary skill in the art at the time of invention to use the address argument as taught by PCI specification into Lakhani's system modified by SD and thereby further allowing an unused bit AD [0] of the address argument AD [31:0] to be used as an address mode field indicator (see PCI specification page 202).

As in claims 23-24 Lakhani and SD do not expressly disclose the claim's aspect associating with the significant bit of a field such as address argument. However PCI specification discloses an address argument AD [31:0] in which the bits AD[0] represent address mode field, The binary values of AD[0] further indicates two address modes

corresponding to accessing data in I/O space and/or memory space. It would have been obvious to one of ordinary skill in the art at the time of invention to use the address argument as taught by PCI specification and thereby further allowing an unused bit AD[0] of the address argument AD[31:0] to be used as an address mode field indicator (see PCI specification page 202). It's further noted that the bit AD [0] can be designated as least significant/most significant bit, and the designation can be based on whether the endianess of the associating logic operates on the data.

Response to Arguments

Applicant's remarks filed 2/28/2008 have been fully considered but they are moot in view of new ground(s) of rejection applied with new reference(s) found.

Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Hyung S SOUGH/

Supervisory Patent Examiner, Art Unit 2188

04/28/08